APPLICATION

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TITLE: DISCRIMINATIVE SOI WITH OXIDE HOLES UNDERNEATH DC SOURCE/DRAIN

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DISCRIMINATIVE SOI WITH OXIDE HOLES UNDERNEATH DC SOURCE/DRAIN

DESCRIPTION

Field of the Invention

[0001] The present invention relates to silicon-on-insulator (SOI) semiconductor integrated circuits (ICs), and more particularly to a selective SOI semiconductor structure that includes body contacts for all SOI devices present therein and a direct current (DC) node diffusion region in which no buried oxide is located directly beneath the DC node.

Background of the Invention

[0002] In semiconductor processing, silicon-on-insulator (SOI) technology is becoming increasingly important since it permits the formation of high-speed integrated circuits. In SOI technology, an insulating material, e.g., a buried oxide, electrically isolates a top Si-containing layer from a bottom Si-containing substrate. The top Si-containing layer, which is oftentimes referred to in the art as the SOI layer, is generally the layer in which active devices such as transistors are formed. Devices formed using SOI technology offer many advantages over their bulk counterparts including, for example, higher performance, absence of latch-up, higher packing density and low voltage applications.

[0003] As SOI devices get smaller, the devices can suffer from a charge buildup in the body of the devices. This charge can cause a number of less than desirable effects including, for example, floating body effects. The floating body effects in SOI devices include a wide range of electrical behaviors resulting directly from the loss of control of the body charge state. Several examples of floating body effects are: (1) threshold voltage Vt that depends on the electrical history of the device (since the history of the

device determines the body charge and effective back bias), (2) reduction of gate voltage control, (3) lowered snapback voltage, (4) degraded sub-Vt slope for static operation, (5) enhanced sub-Vt slope for dynamic operation, and (6) channel current overshoot. To ensure that specific devices do not suffer from these effects, a body contact is typically added as a method to drain off any charge in the body.

[0004] One known approach to provide body contacts is to cut out holes of the blanket buried oxide under the device's channel region so that the body in the device channel can be reached and biased thru the oxide opening. This approach provides a subtractive SOI substrate such as is shown, for example, in FIG. 1A. Specifically, FIG. 1A shows a metal oxide semiconductor field effect transistor (MOSFET) structure that includes a subtractive SOI substrate 10 having a patterned gate conductor 20 located atop a patterned gate dielectric 18. These patterned material layers are located atop the subtractive SOI substrate 10 that includes SOI channel region 16, source/drain regions 15, and buried oxide regions 14; the unlabeled region between the buried oxide regions 14 having boundaries defined by dotted lines represents the cut out buried oxide. The cut out oxide area serves as the body contact in the illustrated structure. Trench isolation region 12 is also shown in FIG. 1A.

[0005] Another approach is to start with the bulk technology and build a buried oxide underneath the Si source/drain. The intended buried oxide region is etched first and oxidized later. This approach provides an additive SOI substrate such as is shown, for example, in FIG. 1B. Specifically, FIG. 1B shows a MOSFET structure that includes an additive SOI substrate 11 having a patterned gate conductor 20 located atop a patterned gate dielectric 18. These patterned material layers are located atop the additive SOI substrate 11 that includes SOI channel region 16, source/drain regions 15, and buried oxide regions 14. Trench isolation region 12 is also shown in FIG. 1B. It is noted that in the structure shown in FIG. 1B the region between the buried oxide serves as the body contact of the field transistor device. Due to the processing of prior art

additive SOI substrates, the Si plate tends to collapse during formation of the buried oxide.

[0006] In both SOI devices shown in FIGS.1A and 1B, the active Si source/drain regions 15 are shielded from the Si substrate (not specifically shown) with a layer of buried oxide 14 underneath. A body contact is located beneath the channel region 16 and the underlying Si-containing substrate.

[0007] In actual IC designs, many source/drain regions are direct current (DC) nodes that do not switch at all. In particular, for the applied voltage VDD and ground GND regions buried oxides are actually undesirable. Moreover, the overall power bussing will miss the stabilization effects from the diffusion capacitance from the devices. For the individual circuits, the supply nodes will be bumped up and down more easily, and slow down the switching. Since the body contacts have to be at a distance away from the buried oxide, prior art layouts tend to be much larger than is necessary.

Summary of the Invention

[0008] In view of the foregoing and other problems of prior art SOI technology, there is a need to provide a selective SOI structure having body contacts for all the devices while excluding the buried oxide that is directly underneath diffusions of DC nodes such as applied voltage Vdd, ground GND, reference voltage Vref, and other like DC nodes. The selective SOI structure of the present invention may be referred to as a discriminative SOI structure since oxide holes are present beneath the DC nodes, while oxide is present beneath the SOI devices active switching source/drain regions.

[0009] The selective SOI structure of the present invention can be used in ICs to enhance the performance of the circuit. Circuit performance enhancement up to 30 % is possible utilizing the selective SOI structure of the present invention. Moreover, the

selective SOI structures of the present invention use an additive process in which the collapse of the Si plate is avoided.

[0010] In broad terms, the selective SOI structure of the present invention comprises:

[0011] a silicon-on-insulator (SOI) substrate material comprising a top Si-containing layer having a plurality of SOI devices located thereon, said SOI devices are in contact with an underlying Si-containing substrate via a body contact region; and

[0012] a DC node diffusion region adjacent to one of said SOI devices, said DC node diffusion region is in contact with said Si-containing substrate, i.e., the DC node diffusion region does not contain an underlying buried oxide region.

[0013] In accordance with the present invention, the DC node diffusion regions contain oxide holes, while the active source/drain regions of the SOI devices contain buried oxide material underneath. The selective SOI structure described above can be employed in various circuit design layouts to provide an IC that has enhanced circuit performance.

[0014] In the selective SOI structure described above, a semiconductor substrate for use in ICs is provided that includes at least an SOI substrate; a DC node diffusion region in said SOI substrate; and a buried insulator material within said SOI substrate, wherein said DC node diffusion region is in contact with an underlying Si-containing substrate of said SOI substrate, i.e., the DC node diffusion region does not include an underlying buried oxide. Instead, an oxide hole is located beneath the DC node diffusion region.

Brief Description of the Drawings

[0015] FIGS. 1A-1B are pictorial representations (through cross sectional views) illustrating a prior art structure containing a subtractive SOI substrate (FIG. 1A) and a prior art structure including an additive SOI substrate (FIG. 1B).

[0016] FIG. 2 is a pictorial representation (through a cross section view) illustrating the selective SOI semiconductor IC of the present invention.

[0017] FIGS. 3A-3F are pictorial representations (through cross sectional views) illustrating basic processing steps that are employed in fabricating the selective SOI substrate of the present application.

[0018] FIGS. 4A-4B are schematics showing complementary metal oxide semiconductor (CMOS) IC design layouts of the prior art (FIG. 4A) and the present invention (FIG. 4B).

[0019] FIG. 5 is schematic showing a complementary metal oxide semiconductor (CMOS) IC design layout of the present invention.

Detailed Description of the Invention

[0020] The present invention, which provides a selective SOI structure and the use thereof in various ICs, will now be described in greater detail by referring to the drawings that accompany the present application. It is noted that the drawings that accompany the present application are not drawn to scale; therefore the invention is not limited to any dimension that may be ascertained from the drawings.

[0021] Reference is first made to FIG. 2, which provides a simple cross sectional view of the selective SOI structure 50 of the present invention. The selective SOI structure

50 of the present invention comprises a silicon-on-insulator (SOI) substrate 52 having a plurality of semiconductor devices 54, such as MOSFETs, located on a surface of the SOI substrate 52. In FIG. 2, two semiconductor devices 54 are provided for illustrative purposes.

[0022] Each semiconductor devices 54 includes a patterned gate conductor 56 located on top of a patterned gate dielectric 58. Source/drain diffusion regions 60 are located within a top Si-containing layer 68 of the SOI substrate 52. A channel region 62 is located beneath each of the semiconductor devices 54. The channel region 62 is bounded on each side by the source/drain diffusion regions 60.

[0023] In accordance with the present invention, the selective SOI structure 50 includes a body contact region 64 that permits contact of the top Si-containing layer 68 of the SOI substrate 52 with an underlying Si-containing substrate 72. No buried insulator oxide 70 is located directly beneath the channel region 62 of each semiconductor device. The presence of the body contact regions 64 obviates the floating body effects mentioned in the background section of the present invention.

[0024] In addition to the above structural features, the structure of the present invention also includes at least one DC node diffusion region 74 that is located within the SOI substrate 52. As shown, the DC node diffusion region 74 lies to the periphery of the MOSFET devices 54 shown in FIG. 2.

[0025] In accordance with the present invention, no buried oxide 70 is located beneath the DC node diffusion region 74. Instead, the DC node diffusion region 74 is in contact with the bottom Si-containing substrate 72 of the SOI substrate 52, i.e., an oxide hole is present beneath the DC node diffusion region 74.

[0026] As indicated above, the SOI substrate 52 includes a top Si-containing layer 68, regions of buried oxide 70 and a bottom Si-containing substrate 72. The term "Si-

containing" as used throughout the present application denotes a semiconductor material that includes at least silicon. Illustrative examples of such Si-containing materials include, but are not limited to: Si, SiGe, SiC, SiGeC, Si/Si, Si/SiC, and Si/SiGeC. The Si-containing material of layers 68 and 72 may be doped or undoped.

[0027] The top Si-containing layer 68 of the SOI substrate 52 typically has a thickness from about 50 to about 200 nm, with a thickness from about 75 to about 100 nm being more typical. The thickness of the bottom Si-containing substrate 72 is typically from about 700 to about 750 μm.

[0028] The buried oxide 70 employed in the present invention can be a crystalline or non-crystalline oxide. The buried oxide 70, which is located beneath the active source/drain diffusion regions 60 of each semiconductor device 54, typically has a thickness from about 30 to about 100 nm.

[0029] The SOI substrate 52 illustrated in FIG. 2 is an additive SOI substrate that is formed utilizing an additive SOI process, which is describe, for example, in co-assigned U.S. Serial No. 10/604,102, filed June 26, 2003, the entire content of the aforementioned U.S. Application is incorporated herein by reference. FIGS. 3A-3F, to be discussed in greater detail hereinbelow, provide a brief description of the process flow that can be employed in the present invention for forming the additive SOI substrate 52.

[0030] The semiconductor devices 54 are formed utilizing conventional complementary metal oxide semiconductor (CMOS) processing steps that are well known to those skilled in the art. For example, the semiconductor devices 54 can be formed by first forming a layer of gate dielectric 58 on an upper surface of the top Si-containing layer 68 of the SOI substrate 52. The term "gate dielectric" is used in the present invention to denote any insulating material, such as an oxide, nitride or oxynitride, that is typically employed as the gate dielectric of an MOSFET. The gate dielectric 58 is formed by a

conventional deposition process such as, for example, chemical vapor deposition (CVD), plasma-assisted CVD, atomic layer deposition, physical vapor deposition or another like deposition process. Alternatively, the gate dielectric 58 can be formed by a thermal oxidation, nitridation or oxynitridation process. The thickness of the gate dielectric 58 is typically from about 1 to about 10 nm.

[0031] After formation of the gate dielectric, a gate conductor 56 is formed atop the gate dielectric. The gate conductor 56 may include any conductive material, including for example, doped polysilicon, conductive elemental metals, alloys of conductive elemental metals, silicides of conductive elemental metals, nitrides of conductive elemental metals, or any combination thereof. A diffusion barrier and/or a dielectric cap may be formed within or atop the gate conductor 56. Gate conductor 56 can be formed by a conventional deposition process such as, for example, CVD, plasma-assisted CVD, evaporation, sputtering, plating or another like deposition process. When polysilicon is employed, the polysilicon gate conductor is a doped material that can be formed in-situ, or by deposition and then ion implantation. The thickness of the gate conductor 56 is typically from about 100 to about 300 nm.

[0032] Following formation of the gate conductor, the gate conductor 56 and typically, the gate dielectric 58 are patterned by lithography and etching. Next, insulating spacers (not shown) are typically formed (by deposition and etching) on the exposed sidewalls of at least the patterned gate conductor 56. Following spacer formation, the source/drain diffusion regions 60 are formed into the top Si-containing layer 68 of the SOI substrate 52 by ion implantation and annealing. The source/drain regions 60 are formed into the top Si-containing layer 68 that has an underlying buried insulator material 70.

[0033] The annealing causes diffusion of the implanted dopants. The extent of the diffusion determines the length of the channel regions 62 in the top Si-containing layer 68 of the SOI substrate 52. The channel regions 62 are positioned such that a body

contact region 64 is present below each of the channel regions 62 such that the semiconductor devices 54 do not exhibit the floating body effects.

[0034] It should be noted that the trench isolation regions 66 are typically formed into the SOI substrate 52 prior to formation of the semiconductor devices 54. The trench isolation regions are formed utilizing the additive SOI process, which will be described in greater detail hereinbelow.

[0035] At the same time as forming the source/drain diffusion regions 60 or at an earlier or later time than source/drain region 66 formation, the DC node diffusion region 74 is formed within the SOI substrate 52 at a location to the periphery of the semiconductor devices 54 and wherein no buried insulator material 70 is present. The DC node diffusion region 74 is formed by ion implantation and annealing. In accordance with the present invention, the DC node diffusion 74 contains no underlying buried oxide 70; therefore it is in contact with the bottom Si-containing substrate 72 of the SOI substrate 52. The DC node diffusion 74 may be a region in which a source voltage can be applied, a region in which a reference voltage can be applied, a ground region or any combination thereof such as, for example, a region in which a source voltage is applied and a region of ground. It is noted that the present invention may include a single DC node diffusion region 74 or a plurality of such regions located within the SOI substrate 52.

[0036] It is again emphasized that the selective SOI structure 50 shown in FIG. 2 includes SOI semiconductor devices 54 having source/drain 60 that are located atop regions of buried oxide 70. To avoid problems caused by floating body effects, the selective SOI structure 50 shown in FIG. 2 has body contact regions 64 beneath the MOSFET device channel 62. Moreover, in the inventive selective SOI structure 50, the DC node diffusion 74 does not include an underlying buried oxide 70 therefore it is in direct contact with the Si-containing substrate 72 of the SOI substrate 52.

[0037] The additive SOI substrate 52 employed in the present invention is fabricated utilizing an additive SOI process such as is described in the previous mentioned application that is incorporated herein by reference. The additive SOI process is exemplified briefly in FIGS. 3A-3F which are now described. FIG. 3A illustrates the initial structure 100 that is employed in fabricating the additive SOI substrate 52 of the present invention. As shown, the initial structure 100 includes a bulk Si-containing substrate 102 having n-doped regions 104 formed therein. The n-doped regions 104 are areas in which the buried insulator material 70 of the SOI substrate 52 will be subsequently formed.

[0038] The n-doped regions 104 are formed utilizing a masked ion implantation process. Annealing may follow the implantation to cause activation and diffusion of the n-type dopant. The bulk Si-containing substrate 102 will become the bottom Si-containing substrate 72 of the additive SOI substrate 52 shown in FIG. 2.

[0039] FIG. 3B shows the structure after a Si-containing layer 106 is formed atop the initial structure 100. The Si-containing layer 106, which serves as the top Si-containing layer 68 of the additive SOI substrate 52 shown in FIG. 2, is formed by an epitaxial growth process.

[0040] FIG. 3C shows the structure after forming a photoresist 116 and a pad stack 108 atop the Si-containing layer 106. The pad stack 108 comprising a nitride layer 112, and an oxide layer 114. Pad stack 108 is formed by deposition, a thermal process or a combination thereof.

[0041] Next, and as shown in FIG. 3D, trench openings 118 are formed into the structure shown in FIG. 3C by first patterning the photoresist 116 by lithography and then transferring the pattern from the photoresist into the pad stack 108 by a first etching step. Following the first etching step, the patterned photoresist is removed and a second etching step is employed to transfer the pattern into the Si-containing layer 106

and then the n-doped regions 104. The second etching step stops atop a surface of the bulk Si-containing substrate 102 that lies beneath the n-doped regions 104.

[0042] A lateral etch is then used to remove the remaining n-doped regions 104 providing the structure shown, for example, in FIG. 3E. Reference numeral 120 denotes the voids created by the lateral etch.

[0043] FIG. 3F shows the resultant additive substrate 52 after filling the voids with an oxide and removing the various layers atop layer 106. Note that the lateral etched and oxide filled areas become the buried insulator 70 of the structure shown in FIG. 2. The oxide within the vertical etched trench becomes the trench isolation regions 66 of the structure.

[0044] The selective SOI structure shown in FIG. 2 containing discriminative oxide holes underneath the DC node diffusion regions 74 can be used in various IC layouts to provide improved IC performance. FIG. 4A shows a prior art IC layout for a standard NAND gate of a standard selective SOI substrate, while FIG. 4B shows the inventive selective SOI structure in the same IC layout. In each drawings, PC denotes the polysilicon conductor that forms the gate of the FET devices, VDD denotes the applied potential, RX denotes the region of active silicon, BX denotes buried oxide, and BXHOLE denotes the buried oxide cut out.

[0045] In the prior art IC layout, BXHOLE is only cut out at the channel region. In the claimed invention, the BXHOLE is expanded into the supply diffusion regions as shown to add another 5 to 10% of performance to the design. The buried oxide ring around the RX boundary is mainly to enhance deep well isolation. For some embodiments, the N+ or P+ spacing can be reduced to zero if they are covered by BX.

[0046] For the additive SOI process, it is critical to avoid buried oxide under supply diffusion regions. On example of such an IC layout is shown in FIG. 5. At the lower

left corner of FIG. 5, a piece of active Si is connecting to the GND supply to three NFETs.

[0047] In FIG. 5, GND BXHOLE and VDD BXHOLE are the DC non-switching nodes of the FET device source/drain regions, underwhich no oxide is formed. The regions without oxide provide the support to the hanging Si plates after the lateral etch. (See, FIG. 3E reference numeral 120). The other DC nodes labeled as VDD and GND serve the same supporting function before the actual underground oxide is formed.

[0048] While the present invention has been particularly shown and described with respect to preferred embodiments thereof, it will be understood by those skilled in the art that the foregoing and other changes in forms and details may be made without departing from the scope and spirit of the present invention. It is therefore intended that the present invention not be limited to the exact forms and details described and illustrated, but fall within the scope of the appended claims.